

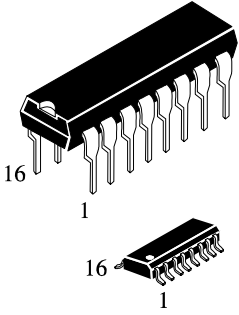
**KK74HC175A**

**Quad D Flip-Flop with  
Common Clock and Reset  
High-Performance Silicon-Gate CMOS**

The KK74HC175A is identical in pinout to the LS/ALS175. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

This device consists of four D flip-flops with common Reset and Clock inputs, and separate D inputs. Reset (active-low) is asynchronous and occurs when a low level is applied to the Reset input. Information at a D input is transferred to the corresponding Q output on the next positive-going edge of the Clock input.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices

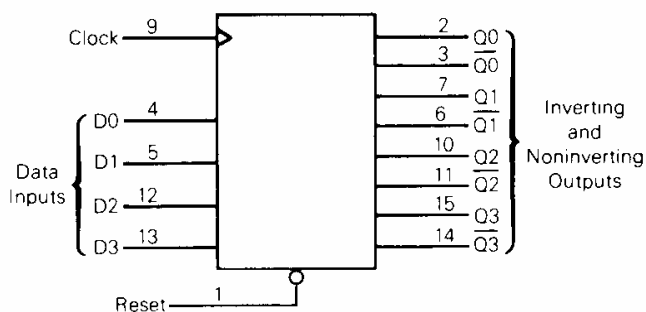


N SUFFIX  
PLASTIC

D SUFFIX  
SOIC

**ORDERING INFORMATION**  
 KK74HC175AN Plastic  
 KK74HC175AD SOIC  
 $T_A = -55^\circ$  to  $125^\circ$  C for all packages

**LOGIC DIAGRAM**





PIN 16 =  $V_{CC}$   
 PIN 8 = GND

**PIN ASSIGNMENT**

RESET	1	16	$V_{CC}$
Q0	2	15	Q3
$\overline{Q0}$	3	14	$\overline{Q3}$
D0	4	13	D3
D1	5	12	D2
$\overline{Q1}$	6	11	$\overline{Q2}$
Q1	7	10	Q2
GND	8	9	CLOCK

**FUNCTION TABLE**

Inputs			Outputs	
Reset	Clock	D	Q	$\overline{Q}$
L	X	X	L	H
H		H	H	L
H		L	L	H
H	L	X	no change	

X = Don't care

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{IN}$	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
$V_{OUT}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{IN}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{OUT}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	$^{\circ}\text{C}$

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/ $^{\circ}\text{C}$  from 65 $^{\circ}$  to 125 $^{\circ}\text{C}$

SOIC Package: - 7 mW/ $^{\circ}\text{C}$  from 65 $^{\circ}$  to 125 $^{\circ}\text{C}$

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
$V_{IN}, V_{OUT}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-55	+125	$^{\circ}\text{C}$
$t_r, t_f$	Input Rise and Fall Time (Figure 1)			ns
	$V_{CC} = 2.0 \text{ V}$	0	1000	
	$V_{CC} = 4.5 \text{ V}$	0	500	
	$V_{CC} = 6.0 \text{ V}$	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range  $\text{GND} \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V   I <sub>OUT</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low - Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V   I <sub>OUT</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		6.0	5.9	5.9	5.9		
		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 4.0 mA   I <sub>OUT</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.7	
6.0	5.48	5.34	5.2				
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>   I <sub>OUT</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		6.0	0.1	0.1	0.1		
		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>   I <sub>OUT</sub>   ≤ 4.0 mA   I <sub>OUT</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.4	
6.0	0.26	0.33	0.4				
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA	6.0	8.0	80	160	μA

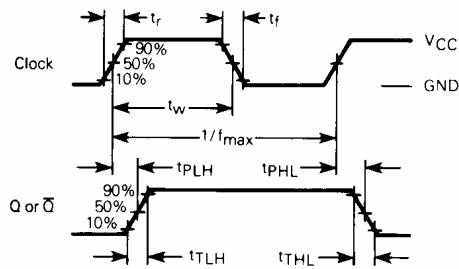
**AC ELECTRICAL CHARACTERISTICS** ( $C_L=50\text{pF}$ , Input  $t_r=t_f=6.0\text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
$f_{max}$	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
$t_{PLH}, t_{PHL}$	Maximum Propagation Delay, Clock to Q or $\bar{Q}$ (Figures 1 and 4)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Reset to Q or $\bar{Q}$ (Figures 2 and 4)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
$t_{TLH}, t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
$C_{IN}$	Maximum Input Capacitance	-	10	10	10	pF

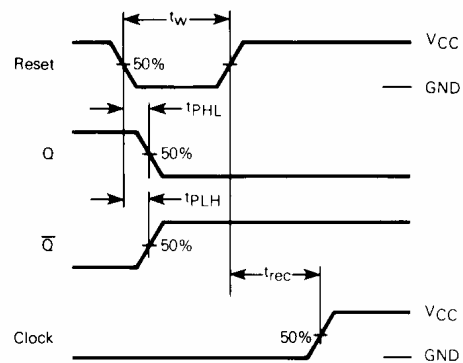
$C_{PD}$	Power Dissipation Capacitance (Per Flip-Flop)	Typical @25°C, $V_{CC}=5.0\text{ V}$			pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	35			

**TIMING REQUIREMENTS** ( $C_L=50\text{pF}$ , Input  $t_r=t_f=6.0\text{ ns}$ )

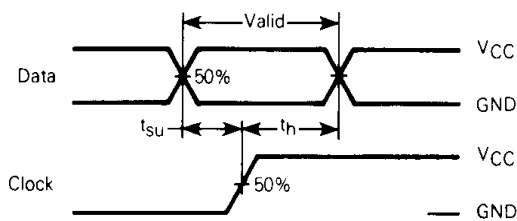
Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
$t_{SU}$	Minimum Setup Time, Data to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
$t_h$	Minimum Hold Time, Clock to Data (Figure 3)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
$t_{rec}$	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
$t_w$	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
$t_w$	Minimum Pulse Width, Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
$t_r, t_f$	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	



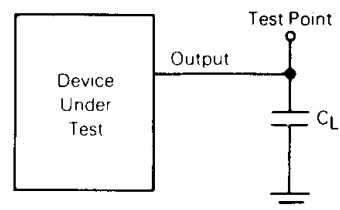
**Figure 1. Switching Waveforms**



**Figure 2. Switching Waveforms**



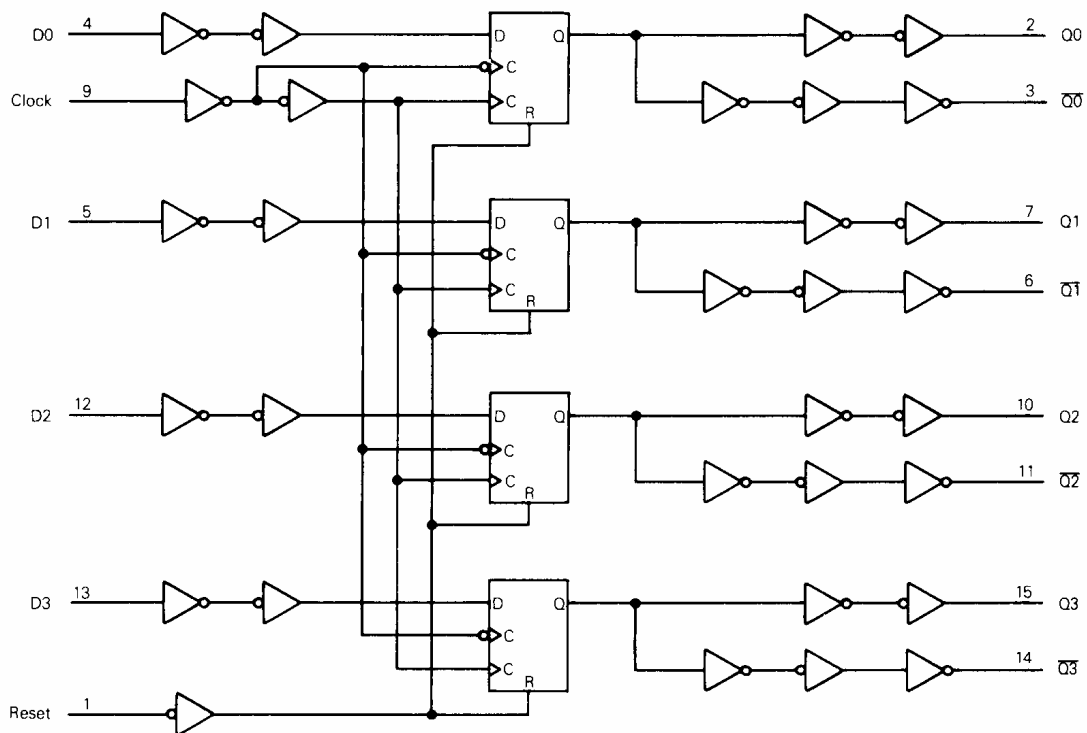
**Figure 3. Switching Waveforms**



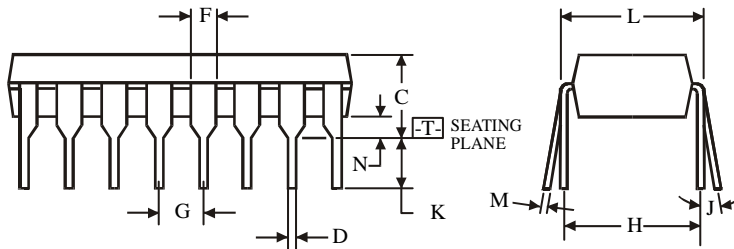
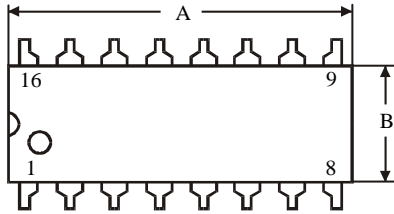
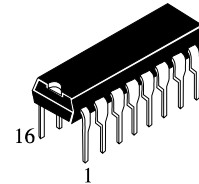
\* Includes all probe and jig capacitance.

**Figure 4. Test Circuit**

**EXPANDED LOGIC DIAGRAM**



**N SUFFIX PLASTIC DIP  
(MS - 001BB)**



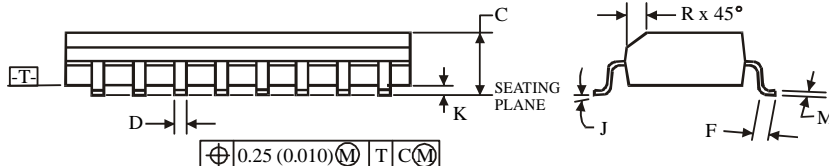
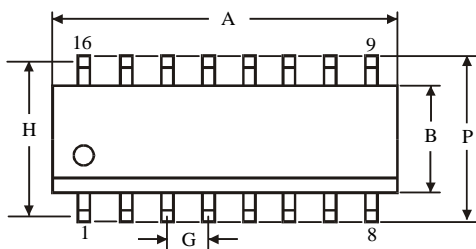
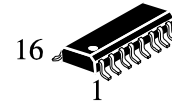
$\oplus 0.25 (0.010) \text{M} \text{T}$

**NOTES:**

- Dimensions "A", "B" do not include mold flash or protrusions.  
Maximum mold flash or protrusions 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	18.67	19.69
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

**D SUFFIX SOIC  
(MS - 012AC)**



$\oplus 0.25 (0.010) \text{M} \text{T} \text{C} \text{M}$

**NOTES:**

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	9.8	10
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5